REMARKS

At the time the current Official Action was mailed, claims 1-37 were pending. In the Official Action, the Examiner rejected claims 1-18, 21-29 and 31-37, and objected to claims 19, 20 and 30. Applicant thanks the Examiner for the indication of allowable subject matter in claims 19, 20 and 30. However, in the present response, Applicant has not amended, cancelled or added any claims because the cited reference is believed to be insufficient to support a *prima facie* case of anticipation, as discussed below in greater detail. As such, claims 1-37 remain pending in the present application. Reconsideration of the application in view of the remarks set forth below is respectfully requested.

Rejection Under 35 U.S.C. § 102 (b)

The Examiner rejected claims 1-18, 21-29 and 31-37 under 35 U.S.C. § 102(b) as being anticipated by Manning et al. (U.S. Patent No. 6,005,816), which is herein referred to as "Manning." Specifically, with regard to the independent claims 1, 14 and 21, the Examiner stated:

> Regarding claims 1, 14, 21, Manning et al. disclose system (Figure 8) comprising:
> a processor (302); and
> a memory device coupled to the processor that comprises:
> a memory array (10); and
> a buffer device (Figure 8) comprising:
> a plurality of comparators (Figure 4, 160), wherein each of the plurality of comparators is adapted to receive a data signal and one of a first signal and a second signal, wherein the second signal is a complimentary signal of the first signal (ABSTRACT, Column 2, lines 20-33); and
> a plurality of two channel comparators adapted to receive a plurality of output signals from the plurality of comparators and to produce a first output signal and a second output signal with the second

output signal being a complimentary signal of the first output signal (Figure 4).

Official Action, pp. 2-3.

Applicant respectfully traverses the rejection. Anticipation under Section 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 U.S.P.Q. 773 (Fed. Cir. 1985). For a prior art reference to anticipate under Section 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). To maintain a proper rejection under Section 102, a single reference must teach each and every element or step of the rejected claim. *Atlas Powder v. E.I. du Pont*, 750 F.2d 1569 (Fed. Cir. 1984). Thus, if the claims recite even one element not found in the cited reference, the reference does not anticipate the claimed invention.

As a preliminary matter, in the rejection, the Examiner only specifically addressed claims 1-18, 21-29 and 31. That is, the Examiner did not specifically address the subject matter recited in each of the claims 32-37. Because the Examiner did not specifically address claims 32-37, Applicant respectfully asserts that the general rejection of claims 32-37 is believed to be deficient in view of 37 C.F.R. § 1.104(c)(2). Applicant respectfully reminds the Examiner of his duties and obligations under 37 C.F.R. § 1.104 and M.P.E.P. § 707.07 and requests that the Examiner clarify the rejection and specifically address the features recited in claims 32-37 in a future non-final Office Action. To further the prosecution of the present application, Applicant has addressed the specific rejection of independent claims 1, 14 and 21 and as it is assumed to be applied to independent claim 32.

The present application is directed to a digital switching technique for detecting data in a semiconductor device. Other switching techniques utilize a single reference voltage, multiple pins, or even complimentary signals, but these techniques are inefficient, increase fabrication costs, or introduce feedback-timing and symmetry issues. *See* Application, p. 3, line 17 – p. 4, line 11. To provide higher performance data sensing, a switching structure or device may minimize the timing and symmetry issues by utilizing a two stages and differential signals. *See id.* at Fig. 3; p. 13, line 21 – p. 16, line 11. The first stage may include multiple comparators, such as comparators 302, 304, 306 and 308, which receive a data signal DATA and one of the voltage timing reference (VTR) signals VTR1 or VTR2, which are complimentary signals with respect to each other. *See id.* at Figs. 3 and 5; p. 14, line 8 – p. 15, line 15; p. 19, line 11- p. 21, line 22. The second stage may include multiple two-channel comparators, such as two-channel comparators 310 and 312, which receive the output signals from each of the first stage comparators 302, 304, 306 and 308 and provide complimentary output signals. *See id.* at Figs. 3 and 6; p. 15, line 17 – p. 16, line 11; p. 22, line 1- p. 26, line 4. Accordingly, independent claims 1, 14, 21 and 32 recite subject matter relating to the use of these various stages for detecting data.

In contrast to the present application, the Manning reference discloses a sense amplifier that amplifies data signals in either a normal mode or an altered mode. *See* Manning, col. 5, lines 12-27. As discussed in the Manning reference, a sense amplifier circuit 100 receives two data signals that are provided to transistors in a quad configuration. *See id.* at Figs. 1-3, col. 2, line 65 to col. 3, line 15; col. 4, lines 9-14. Because this configuration is only capable of amplifying signals that are differential, it is not cost effective. *See id.* at col. 4, line 58 – col. 5, line 1-10.

Accordingly, Manning discloses using a mode control circuit 170 between the sense amplifiers 100a, 100b, 100c, and 100d. *See id.* at Fig. 4, col. 6, lines 13-36. That is, the sense amplifier 160 of Manning simply utilizes four sense amplifier circuits 100a, 100b, 100c, and 100d coupled to the mode control circuit 170 to select between two modes.

In the rejection of claims 1, 14 and 21 and as it is assumed to be applied to independent claim 32, the Examiner asserted that the Manning reference discloses all of the subject matter recited in the claims. Specifically, the Examiner asserted that "the plurality of comparators" recited in each of the independent claims corresponds to the sense amplifier 160 of Manning and the "plurality of two channel comparators" recited in each of the independent claims corresponds to items shown in Figure 4 of Manning. However, despite the Examiner's assertions, the Manning reference fails to disclose or suggest all of the claimed features. For example, the Manning reference fails to disclose "a plurality of two channel comparators adapted to receive a plurality of output signals from the plurality of comparators and to produce a first output signal and a second output signal with the second output signal being a complimentary signal of the first output signal," as recited in claims 1, 14 and 21. Similarly, the Manning reference fails to disclose "receiving each of the plurality of output signals at each of a plurality of two channel comparators" and "generating a first output and a second output from the plurality of two channel comparators, wherein the second output signal is a complimentary signal of the first output signal," as recited in claim 32. Accordingly, Applicant respectfully submits that the Manning reference fails to anticipate the claims.

The Manning reference does not disclose or suggest two-channel comparators that receive output signals from multiple comparators and that produce two complimentary output signals. The Examiner asserted that the "plurality of comparators" recited in the present claims corresponds to the sense amplifier 160 of Manning and that the "plurality of two channel comparators" of the claims corresponds to items shown in Figure 4 of Manning. As noted above, the sense amplifier 160 of FIG. 4 is described as four sense amplifier circuits 100a, 100b, 100c and 100d that are coupled to mode control circuitry 170. *See* Manning, Fig. 4, col. 6, lines 13-36. As specifically described in the reference, these sense amplifier circuits 100a, 100b, 100c and 100d are simply four different conventional sense amplifier circuits that receive a pair of input signals. *See* Manning, Figs. 2 and 4, col. 3, lines 7-15; col. 6, lines 13-19. Further, the Manning reference does not even disclose a two-channel comparator, much less two-channel comparators that receive output signals from multiple comparators and that produce two complimentary output signals. At best, the Manning reference describes two one-channel comparators that each provide a signal output signal to a mode control circuit and one of two different one-channel comparators. As such, the Manning reference fails to disclose the claimed subject matter.

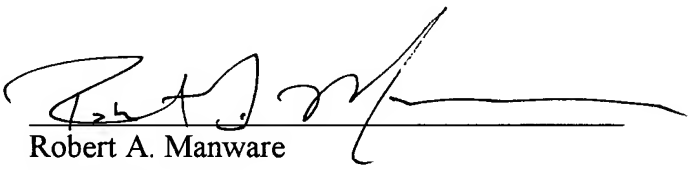
Because the Manning reference fails to disclose all the recited features of the instant claims, it cannot possibly anticipate the claimed subject matter. As such, Applicant respectfully requests withdrawal of the Examiner's rejections and allowance of claims 1-18, 21-29 and 31-37.

Conclusion

In view of the remarks set forth above, Applicant respectfully requests reconsideration of the Examiner's rejections and allowance of all pending claims 1-37. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Date: March 21, 2005



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